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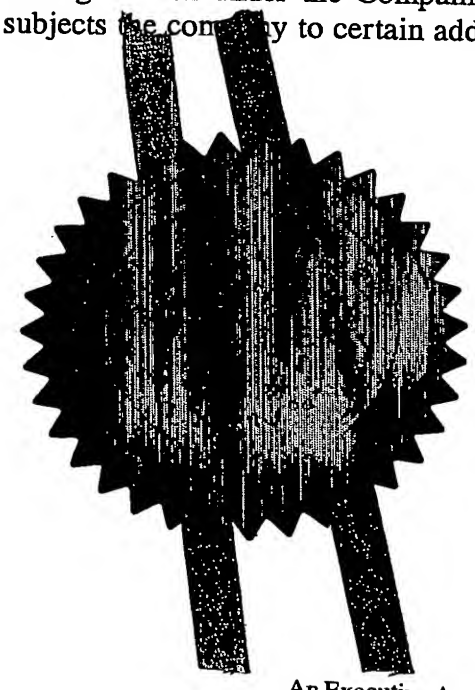

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Dated 30 April 2004

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The Patent Office

Cardiff Road
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NP9 1RH

1. Your reference — P3161 GB PRO

2. Patent application number *(The Patent Office will fill in this part)* — 0308086.8

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

AOTI OPERATING COMPANY, INC.
131 NW HAWTHORNE AVENUE
SUITE 207
BEND, OREGON 97701, US

Patents ADP number *(if you know it)* 08113805002

If the applicant is a corporate body, give the country/state of its incorporation — DELAWARE, USA

4. Title of the invention — OVERLAY ALIGNMENT MARK

5. Name of your agent *(if you have one)* — NOVAGRAAF PATENTS LIMITED

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

THE CRESCENT
54 BLOSSOM STREET
YORK YO24 1AP

Patents ADP number *(if you know it)* — 08299166001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

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Description	9
Claim(s)	
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Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	
Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature NOVAGRAAF PATENTS LIMITED Date 08/04/2003

12. Name and daytime telephone number of person to contact in the United Kingdom PETER WILSON (DR) 01904 610586

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Overlay Alignment Mark

The invention relates to overlay metrology during semiconductor device fabrication, and in particular to an overlay alignment mark to facilitate alignment and/ or measure the alignment error of two layers on a semiconductor wafer structure, or different exposures on the same layer, during its fabrication.

Modern semiconductor devices, such as integrated circuits, are typically fabricated from wafers of semiconductor material. In particular, a wafer is fabricated comprising a succession of patterned layers of semiconductor material.

Overlay metrology in semiconductor device fabrication is used to determine how well one printed layer is overlaid on a previously printed layer. Close alignment of each layer at all points within the device is crucial for reaching the design goals and hence the required quality and performance of the manufactured device. It is consequently of importance for the efficiency of the manufacturing process that the any alignment error between two patterned layers on a wafer, especially successive patterned layers can be measured quickly and accurately. It is similarly important to be able to measure any alignment error between successive exposures in the same layer, and where reference is made herein for convenience to two layers it will be understood where appropriate to apply equally to two exposures in the same layer.

Misregistration between layers is referred to as overlay error. Overlay metrology tools are used to measure the overlay error. This information may be fed into a closed loop system to correct the overlay error.

Current overlay metrology employs optically readable target patterns, printed onto the successive layers of a semiconductor wafer during fabrication. The relative displacement of two successive layers is measured by imaging the patterns at high magnification, digitizing the images, and processing the image data using various known image analysis algorithms to quantify the alignment.

The pattern of the target mark may be applied to the wafer by any suitable method. In particular, it is often preferred that the mark is printed onto the wafer layers using photolithographic methods. Typically, this or some other suitable technique is used to apply overlay target marks on each of two wafer layers to be tested to enable alignment information to be measured which is representative of the alignment of the layers. Accuracy of layer alignment should correspond to accuracy of circuit pattern alignment within the fabricated wafer.

Current overlay metrology is normally practised by printing targets with rectangular or other symmetry. For each measurement two targets are printed, one in the current layer and one in a previous layer, or one in association with each pattern in a common layer. The choice of which previous layer to use is determined by process tolerances. The two targets have a nominally common centre, but are printed with different sizes so that they can be differentiated. Normally, but not always, the target printed in the current layer is the smaller of the two targets. An overlay measurement in such a system is the actual measured displacement of the centres of the two targets.

Current preferred practice is that the size of the targets is designed such that both can be imaged simultaneously by a bright-field microscope. The resolution limit of such a microscope determines that the larger of the two targets is typically a 25μm square on the outside. This arrangement permits capture of all of the necessary data for the performance of the measurement

from a single image, and allows overlay measurement tools to make measurements at a rate of one in every two seconds or less.

Such systems are widely and effectively used. However a problem is introduced by the size of the targets, which can make up a significant fraction of the space available in the scribe area surrounding the devices being fabricated. Any automated system used in a production environment must use pattern recognition in order to locate the targets for measurement. Space limitations in the scribe area mean that many similar targets will be printed in close proximity, allowing the possibility that the wrong target will be located and measured. Moreover many of the newer measurement structures do not provide an easy pattern recognition target as there is no isolated well-resolved image in resist However the size of the target cannot be reduced too much, since accurate measurement requires that the measured features are not significantly smaller than the resolution of the microscope system, and achieving good precision requires that as many as possible of such features are visible in the image.

It is an object of the invention to provide an overlay mark mitigating some or all of these advantages, in particular a mark incorporating modifications to existing mark designs to increase accuracy of mark identification without detracting significantly from subsequent accuracy of overlay error measurement.

In accordance with the present invention in a first aspect a recognition key is provided for use in association with an overlay mark for determining the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure. Such as a mark, as will be familiar, comprises a first mark portion associated with a first layer or pattern as the case may be and a

second mark portion associated with a second layer or pattern as the case may be such that optical imaging of the alignment between the first and second mark portions is indicative of alignment therebetween. In accordance with the invention an identification portion for use with such a first mark portion comprises a simple optically readable mark divided into a small number of pattern areas in each of which areas a marking may be present or absent, the pattern of such markings providing a unique identification key so as to serve to identify the first mark portion.

The first mark portion serves as the primary overlay alignment mark, the second mark portion as a reference mark. Alignment and reference marks each including a suitable pattern of overlay test structures of any suitable design which will be familiar to the skilled person are then compared and imaged in familiar manner. An identification portion in accordance with the invention is associated with the alignment mark and gives a simple digital identification of the alignment mark, ensuring the correct mark is selected. The identification portion thus acts as a pattern recognition key.

A similar identification portion may be associated with other alignment marks on a wafer, whereby the invention comprises an overlay mark system for the whole wafer ensuring the correct marks are selected at all times. The probability of locating the wrong overlay mark can be reduced by varying the pattern in adjacent marks, increasing the distance to a potentially confusing pattern recognition key.

In accordance with the invention in a further aspect, an overlay mark system for determining the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises a first mark portion, a second mark portion, and an identification portion as above defined. In

particular, the identification portion is laid down with the first mark portion, for example at the same time and for example on the same layer. The identification portion is conveniently located proximal to the first mark portion, for example comprising a part thereof.

The recognition key comprises a simple pattern exhibiting a small number of discrete alternative shapes to give a digital identifier. The pattern is adapted to be optically readable by standard imaging equipment at the same time as the primary alignment mark is imaged, requiring no major equipment modification and only minimal modification to image analysis. The recognition key is preferably laid down by the same process as the primary mark, for example employing photolithographic techniques. However, the pattern making up the recognition key is designed to be optically imaged for recognition purposes only, and not for determination of alignment differences. The structure can accordingly be made from structural element(s) which optimise this aspect, and might therefore be substantially larger than the structures making up the primary alignment mark.

The recognition key pattern comprises a small number of pattern areas, for example between four and eight, in each of which areas a marking may be present or absent, the pattern of such markings thus providing the unique identification. In particular, in each pattern area a marking is either substantially entirely present or substantially entirely absent. The arrangement of which pattern areas are present and which are absent gives the unique key. For example, for simplicity it might be preferable if a mark is absent in a single pattern area.

Preferably, the recognition key pattern has a generally square or rectangular outline, to correspond with the generally square or rectangular symmetry of the primary mark. In particular, the horizontal and vertical directions of such

a square or rectangular outline correspond to the horizontal and vertical directions of a similarly square or rectangular overlay mark, and in use with the x and y directions of symmetry in the optical imaging apparatus. As a consequence of this geometry, each pattern area is similarly preferably square or rectangular. The recognition key pattern then preferably comprises a linear or two-dimensional array of such pattern areas, for example consisting of between one and four such areas in each of a row and column direction, corresponding in use to the x and y directions in the optical imaging apparatus.

Each pattern area preferably has dimensions of between 1 and 4 μm, and particularly preferably comprises a 1 μm square. All pattern areas making up the recognition key pattern are preferably identically sized and shaped.

In particular, the key pattern comprises a square or rectangular area sub-divided into a two dimensional array of square or rectangular pattern areas. This gives a highly readable identification mark, maintaining the square or rectangular symmetry of many of the alignment marks with which it is intended to be used, and accordingly easily readable by the imagining equipment. Suitable overall pattern dimensions are from 2 to 8 μm, allowing pattern area dimensions of 1 to 2 μm for ease of imaging. In particular pattern areas are 1 to 2 μm squares.

In a particular embodiment the recognition key pattern comprises a square divided into four equal sub-square pattern areas as above described. Each sub-square pattern area is either present or absent in the recognition key pattern. Mostly preferably, the recognition key pattern comprises a generally L-shaped mark, wherein there are four such sub-square pattern areas in one of which a mark absent. The mark provides four distinct patterns (dependent upon the

orientation of the L-shape) which are easily readable and distinguished. This is sufficient for many purposes.

It is well known that optimal performance depends on measurement being centred on the optic axis of the imaging device. Overlay marks are usually symmetric about this centre, with the overlay error being the measured displacement of the centres. Conveniently, to avoid introducing asymmetry the recognition key may be located at the centre. Alternatively, a plurality of recognition keys are provided away from the centre in locations maintaining the rotational symmetry of the overlay mark.

In a further aspect of the invention, a method of facilitating identification of alignment overlay mark in an overlay mark system for determining the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of semiconductor structure comprises the steps of:

laying down of an alignment mark portion associated with a first layer or pattern as the case may be; and additionally

laying down in association with the said mark portion an identification portion comprising a simple optically readable mark divided into a small number of pattern areas in each of which areas a marking may be present or absent, the pattern of such markings providing a unique identification key so as to serve to identify the alignment mark portion.

The alignment overlay mark is of any suitable design such as will be well known in the art, adapted to be used with a second reference mark portion associated with a second layer or pattern as the case may be such as optical imagining of the alignment between the first and second marked portions is indicative of alignment there between. The identification portion comprises a

recognition key as above described. This is preferably laid down simultaneously with the alignment overlay mark using the same fabrication method, for example by photolithography, as will be familiar to those skilled in the art.

In a further aspect of the invention, a method of determining the relative position between two or more lays of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises the steps of:

laying down a first alignment mark portion in association with a first layer or pattern as the case may be;

laying down a second reference mark portion in association with a second layer or pattern as the case may be;

laying down in association with the said alignment mark portion, preferably simultaneously therewith, an identification portion comprising a simple optically readable mark a simple optically readable mark divided into a small number of pattern areas in each of which areas a marking may be present or absent;

optically imaging the identification portion, collecting and digitizing the image and numerically analysing to obtain information relating the pattern of such markings so as to identify the first mark portion;

optically imaging the first and second mark portions, collecting and digitizing the image and numerically analysing the image data to obtain a quantified measurement of the misalignment of the first and second mark portions.

Each mark portion is preferably laid down by a photolithographic process. Optical imaging of mark is preferably carried out using bright field microscopy. Other preferred features of the methods will be understood by analogy with the foregoing.

The invention will now be described by way of example only with reference to figure 1 of the accompanying drawings, which is a plan view of a preferred embodiment of identification recognition key in accordance with the invention.

Figure 1a shows a basic recognition key in accordance with the invention in top plan view. Increasingly, new measurement structures do not provide an easy pattern recognition target as there is no isolated well-resolved image in the resist. The key comprises a specific mark printed in the resist layer. The mark consists of a 2 μm square mark area subdivided into a two by two array of 1 μm square pattern areas. Three of these are covered by the mark material and one absent. The effect is to produce a key comprising a 2 μm square from which one corner is omitted, giving a general L-shape.

Any corner may be omitted, allowing four unique pattern recognition targets to be created as illustrated in figure 1b. The simplicity of the design makes this easy to image, and easy to distinguish between the four targets, so that the key provides a clear digital identifier of a given overlay mark with which it is associated, and greatly assists in ensuring the correct overlay mark is imaged. Overlay targets can be positioned nearby but will be safe from pattern recognition error if the keys are different. The probability of locating the wrong target can be reduced by varying the omitted corner in adjacent targets, increasing the distance to a potentially confusing pattern recognition key.

Figure 1a

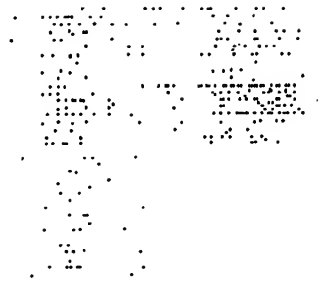

Figure 1b